REMARKS

Applicant would like to thank the Examiner for the careful consideration given the present application. The application has been carefully reviewed in light of the Office action, and amended as necessary to more clearly and particularly describe the subject matter which applicant regards as the invention.

The Examiner rejected claims 1-3 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant notes that claim 1 has been amended and, thus, respectfully requests removal of the rejection.

The Examiner rejected claims 1 and 2 under 35 U.S.C. 103(a) as being unpatentable over Okura et al., U.S. Pat. Pub. No. 2003/0052400 in view of Applicant's admitted prior art (hereinafter "AAPA"). The Examiner's rejection is traversed for the following reason.

In regards to claim 1, Applicant discloses a module structure for a semiconductor device. The module structure includes a high-resistance layer of a first conductive type, a base layer of a second conductive type formed in an upper part of the high-resistance layer, an emitter region of a first conductive type formed in an upper part of the base layer, whereby the emitter region includes an emitter electrode. An insulated gate electrode is located adjacent to the base layer. The module structure further includes a guard ring part formed around a cell region including the emitter region and does not extend onto an upper part of the cell region. The guard ring part includes a semiconductor layer of a second conductive type disposed on an upper part of the high resistance layer of the first conductive

type and located around the emitter region, an insulating layer formed on an upper part of the semiconductor layer of the second conductive type, and a passivation layer covering the insulating layer without covering the cell region whereby the passivation layer is disposed in a non-contact relation to the upper heat-sinking part. The passivation layer does not extend over the cell region, and thus, a gap exists between the passivation film and the heat-sinking part. The gap allows for thermal expansion of both the upper heat-sinking part and the passivation film thereby eliminating thermal stresses between layers in the semiconductor element. A buffer layer of a first conductive type is formed on an underside of the high-resistance layer and a collector layer of the second conductive type is formed on an underside of the buffer layer. A collector electrode connected to the collector layer. One end of a metal flat plate, which is an upper heat-sinking part, is connected to the emitter electrode.

Okura discloses a semiconductor device that has a heat sink soldered to one surface of the semiconductor element and a heat sink soldered to the opposite surface of the semiconductor element. Accordingly, Okura does not teach all the features, for which it is cited, of claim 1. More specifically, Okura does not teach "the passivation layer being disposed in a non-contact relation to the upper heat-sinking part."

Rather, referring to paragraphs [0068] - [0075] and to FIG 8 of Okura, Okura teaches a semiconductor element 1 that includes a p collector layer 102, an n^- drift layer 103 grown on the collector layer 102, a p layer 104 formed on the n^- drift layer 103, and an n^+ emitter region 105 formed in the p layer 104. An emitter electrode 14 is formed so as to make contact with both the emitter region 105 and the p layer 104.

A back electrode 113 is formed on the back side of the semiconductor element 1 whereby a back side heat sink 12 is bonded to the back electrode 113 with solder 5. Referring now to paragraph [0049] and to FIG. 1, Okura further discloses a gate wiring layer 2 formed on the surface of the semiconductor element 1 and a protective (passivation) film 3 formed to cover the wiring layer 2. Paragraph [0049] further discloses a heat sink block 4 bonded to the protective film 3 with solder 5. Further, FIG. 1 clearly shows that the heat sink 4 is in contact, via the solder 5, with the protective film 3. Thus, there does not exist a non-contacting relation between the heat sink 4 and the protective film 3 (passivation layer), as required by claim 1 of the present invention. Therefore, Okura does not teach a non-contact relation between the passivation layer and the heat sink.

Based on the foregoing, it is apparent that Okura does not teach all the features of claim 1, for which it is cited. Thus, reconsideration and withdrawal of the rejections of claim 1 based upon Okura are hereby requested.

Further, in regards to AAPA, Applicant submits that AAPA does not correct or eliminate the deficiencies of the primary reference, Okura. Referring to FIGS. 5 and 6 in AAPA, AAPA does not teach an upper heat sink. Thus, AAPA does not correct or eliminate the deficiencies of Okura. Therefore, Applicant submits that claim 1 is allowable over the proposed combination of the references.

Claim 2 depends from claim 1, thus, all arguments pertaining to claim 1 are equally applicable to claim 2 and are herein incorporated by reference.

The Examiner rejected claim 3 under 35 U.S.C. 103(a) as being unpatentable over Okura et al., U.S. Pat. Pub. No. 2003/0052400 and Applicant's admitted prior art (hereinafter "AAPA") further in view of Hirano et al., U.S. Pat. Pub. No.

2003/0122232. The Examiner's rejection is traversed for the following reason.

Claim 3 depends from claim 1, thus, all arguments pertaining to claim 1 are equally applicable to claim 2 and are herein incorporated by reference.

Further, Applicant submits that Hirano does not correct or eliminate the deficiencies of the primary reference, Okura, as they relate to claim 1. Hirano discloses a semiconductor power device that includes a semiconductor element 11, a lower heat sink 13, and an upper heat sink 14. Hirano, however, does not disclose or suggest that the upper heat sink 14 does not contact a protective film in the semiconductor element 1. Thus, Hirano does not correct or eliminate the deficiencies of Okura, as they relate to claim 1. Therefore, Applicant submits that claim 3 is allowable over the proposed combination of the references.

In light of the foregoing, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in a condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 18-0160, our Order No. SHM-16693.

Respectfully submitted,

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